REMARKS

Claims 9-13 and 15-18 are pending in the application upon entry of the amendments. Claims 9, 17, and 18 have been amended by incorporating the contents of a dependent claim therein. Claim 14 has been cancelled. Since the amendments do not require further searching, place the application in condition for allowance, and/or remove issues in the event of an appeal, entry is respectfully requested. Favorable reconsideration in light of the amendments and the remarks which follow is respectfully requested.

The Amendments

The claims have been amended to indicate the type of devices for the ESD protection; specifically, to disclaim nonvolatile memory devices where the word lines are spaced apart greater than 1 μm. As a result, unnecessary confusion with Fliesler et al Diaz et al, Reisinger, and Wilson et al (cited below) is avoided.

The Novelty Rejection

Claims 9, 10, and 15 have been rejected under 35 U.S.C. § 102 over Fliesler et al. Fliesler et al relates to a nonvolatile memory made by double implanting transistors in the peripheral region. In Column 2, Fliesler et al mentions providing a spacer oxide about the gate in the peripheral region. However, Fliesler et al clearly fails to disclose, teach or suggest that the spacer oxide formed about the gate is formed BEFORE heavy implanting takes place. Moreover, Fliesler et al clearly fails to disclose, teach or suggest that the core region contains word lines connecting the memory cells that are spaced apart by about 1 μm or less. Since Fliesler et al fails to disclose each and every feature of the claims, Fliesler et al cannot anticipate claims 9, 10, and 15.

The Obviousness Rejections

Claims 11 and 16 have been rejected under 35 U.S.C. § 103 over Fliesler et al in view of Diaz et al. Claims 12 and 13 have been rejected under 35 U.S.C. § 103 over Fliesler et al in view of Reisinger. Claim 14 has been rejected under 35 U.S.C. § 103 over Fliesler et al in view of Reisinger further in view of Wilson et al. Claims 17 and 18 have been rejected under 35 U.S.C. § 103 over Fliesler et al in view of Diaz et al.

The deficiencies of Fliesler et al are highlighted above. To address the word line spacing requirements of the claimed invention, the Examiner cites Wilson et al. Wilson et al relates to various aspects of metallization, such as aluminum, tungsten, and copper. However, in non-volatile memory devices, word lines are not made of conductive metal, but instead of semiconductive polysilicon. Thus, the teachings of Wilson et al are not applicable to word line formation in non-volatile memory devices. This is because Wilson et al is directed to metal interconnects in DRAMs, which are very different from polysilicon word lines.

At best, one could possibly argue that one might use the teachings of Wilson et al for guidance in making metal contacts with polysilicon word lines in a non-volatile memory device. But this is very different from arranging the polysilicon word lines themselves. One skilled in the art would not have been motivated by Fliesler et al and Wilson et al to form a non-volatile memory device with a core region containing word lines connecting the memory cells that are spaced apart by about 1 μm or less.

Reisinger is cited for the proposition of describing SONOS devices. Although Reisinger mentions SONOS devices, Reisinger fails to cure the deficiencies of Fliesler et al. In particular, Reisinger fails to teach or suggest a core region containing word lines connecting the memory cells that are spaced apart by about 1 μm or less. Diaz et al discusses ESD in CMOS technologies. Diaz et al fails to teach or suggest a non-volatile memory device with a core region containing word lines connecting the memory cells that are spaced apart by about 1 μm or less. Accordingly, Diaz et al fails to cure

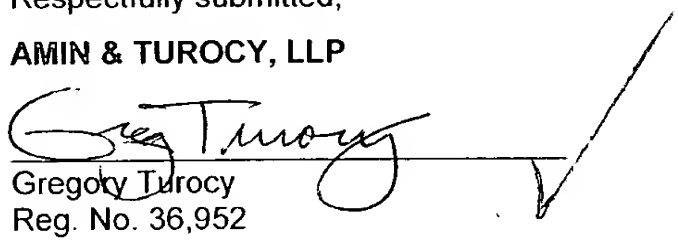
the deficiencies of Fliesler et al. Therefore, for these additional reasons, the claims are unobvious and therefore patentable.

Should the Examiner believe that a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to our Deposit Account No. 50-1063.

Respectfully submitted,

AMIN & TUROCY, LLP



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VERSION OF AMENDMENTS WITH MARKINGS TO SHOW CHANGES

In the Claims:

Please amend the claims in the below-indicated manner.

9. (Twice amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, heavily doping source and drain regions for the electrostatic discharge protection transistors.

17. (Amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1 x 10^{11} atoms/cm^2 to about 1 x 10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 1 x 10^{14} atoms/cm^2 to about 1 x 10^{16} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

18. (Amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1 x 10^{11}

atoms/cm^2 to about 1 x 10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, masking the core region and heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 5 x 10^{14} atoms/cm^2 to about 7 x 10^{15} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

Please cancel claim 14 without prejudice.